

### REMARKS

Claims 1-3 and 5-24 are pending. Claim 25 has been canceled. Claims 17, 18, 20, 21 and 24 have been amended to clarify the subject matter. No new matter has been added.

#### Claim Rejections 35 USC §103

Claims 1, 2, 5-7, 9-11, 14-21, and 23 have been rejected as being unpatentable over Fukutomi et al. in view of Moden. However, the present claimed invention is not obvious over these cited prior art at least for the following reasons.

Claim 1 recites as follows:

1. (Previously Presented) A semiconductor device comprising:

a plurality of conductive paths electrically separated from one another by a trench;

a first conductive path of said plurality of conductive paths, having a die pad shape;

a semiconductor chip disposed over said first conductive path; **said first conductive path coupled to said semiconductor chip through a thermally conductive material;**

a second conductive path disposed peripherally around said semiconductor chip, having a bonding pad shape;

a third conductive path having a shape of an external connecting pad and coupled to said second conductive path, **said third conductive path being disposed underneath said semiconductor chip and coupled to said semiconductor chip through an insulating material;**

connecting means for electrically connecting said semiconductor chip to said second conductive path;

insulating resin covering said semiconductor chip, filling in the trench, and integrally supporting the semiconductor chip and the conductive paths with a bottom surface of the paths exposed. (Emphasis added.)

The above bolded features are not taught or suggested by the combined cited prior art references. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Fukutomi et al. in view of Moden does not show a structure as claimed in claim 1 where the first conductive path, which is disposed underneath the semiconductor chip, is coupled to the semiconductor chip through a thermally conductive material, and the third conductive path, also disposed underneath the semiconductor chip, is coupled to the semiconductor chip through an insulating material.

Fukutomi et al. shows a die-bonding material 66 bonding the chip 65 to the wiring patterns 63 (see Fig. 22c). The Examiner alleges Fukutomi et al. teaches the silver paste/thermally conductive paste or an insulating tape/adhesive between *the chip and the die pad* in column 9, line 13, and column 15, lines 13 to 15 and line 65. This is not correct. The correct reading of the above passages indicate that the sliver paste 4 or 4' is used to bond the LSI chip 3 directly on the copper foil 1 (see Fig. 1 and Fig. 13c); and a polyimide adhesive 28 is used to attach a separately prepared stainless steel frame 22 (see Fig. 16b), which is not the semiconductor chip.

Moden also fails to teach the above bolded feature. In fact, Moden does not teach anything that corresponds to the first conductive path.

That is, none of the cited references show two different conductive paths underneath the semiconductor chip with **one path coupled to the chip through a thermally conductive material and another path coupled to the chip through an insulating material**.

Claims 2, 3, 5 to 13 depend on claim 1 directly or indirectly. Therefore, these claims are also unobvious at least for the same reason as claim 1.

Claim 14 recites:

14. (Previously Presented) A semiconductor device comprising:

a plurality of conductive paths electrically separated from one another by a trench;

a semiconductor chip connected with at least one of said conductive paths through a thermal conductive material; and

insulating resin which covers said semiconductor chip, is embedded in the trench among said plurality of conductive paths and integrally supports the conductive paths, rear surface of which are at least partially exposed from the insulating resin,

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**wherein at least another one of said conductive paths is disposed at a periphery of said semiconductor chip and extends underneath the chip and coupled to the chip through an insulating material to form an external terminal.** (Emphasis added.)

Because claim 14 has similar limitations as claim 1, claim 14 would not have been obvious to a person of ordinary skill in the art at least for the same reason as claim 1. That is, the bolded features above are not disclosed, taught, or suggested by the cited prior art references.

Claims 15 and 16, which depend on claim 14, are also unobvious at least for the same reason as claim 14.


Claim 17 has similar features as claim 1. Thus, at least for the same reasons as claim 1, claim 17 are not obvious. Dependent claims 18 to 24 are not obvious at least for the same reason as claim 17.

For the forgoing reasons, all pending claims are believed to be allowable over the cited art.

Enclosed is a check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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